APPARATUS AND METHOD FOR STATE SELECTABLE TRACE STREAM GENERATION

Abstract of the Invention

A trace test and debug system for a target processor generates a program counter trace stream, a timing trace stream and a data trace stream. The target processor has three states, a program code execution state, an interrupt service routine code execution state, and a state where code execution is halted. The trace streams can be controlled so that the timing trace stream can be generated or excluded during the code execution halts. Similarly, when the timing trace stream is enabled for the interrupt service routine(s), the program counter and data trace streams can be selectively generated or excluded. The contents of the pipeline flattener can be held or flushed code execution halt depending on whether the pipeline is unprotected or protected. When the contents of the pipeline flattener are held during a code halt, the program counter trace stream and data trace stream is halted even if the timing trace stream remains active. When the contents of the pipeline flattener are flushed, the program counter and data trace streams are continued into the period of the code execution halt.